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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/721,331 | 11/26/2003 | Kenji Wada | 109802.01 | 8385 |

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| EXAMINER | |
|---|---|
| DOTY, HEATHER ANNE | |
| **ART UNIT** | **PAPER NUMBER** |
| 2813 | |

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/721,331 | WADA, KENJI |
| | Examiner | Art Unit |
| | Heather A. Doty | 2813 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-8,12 and 13* is/are rejected.

7)☒ Claim(s) *9-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/891,407.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blocker (U.S. 3,969,745) in view of Hatada et al. (U.S. 4,494,688).

Regarding claim 5, Blocker teaches a method to manufacture a semiconductor device, comprising preparing a semiconductor wafer including a chip forming section having an electrode (**10a** in Fig. 3); forming a first through hole in the electrode (**10e** in Fig. 3; column 3, lines 42-46); forming a second through hole penetrating the semiconductor wafer and coaxial to the first through hole, the second through hole communicating with the first through hole (hole through wafer **13** in Fig. 3); and forming a conduction layer (**10** in Fig. 3) that extends via the first and second through holes from a first surface of the semiconductor chip forming section on which the electrode is formed to a second surface opposite the first surface, the conduction layer being electrically connected to the electrode (see Fig. 3).

Blocker does not teach preparing a semiconductor wafer including a plurality of semiconductor chip forming sections each having an electrode.

Hatada et al. teaches that it is known to prepare a semiconductor wafer including a plurality of semiconductor chip forming sections each having an electrode in the pursuit of miniaturization of integrated circuits (column 1, lines 12-18).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to manufacture a semiconductor device according to the method taught by Blocker and further fabricate a plurality of such devices, each on its own semiconductor ship forming section with an electrode, as taught by Hatada et al. is common in the semiconductor device processing arts. The motivation for doing so at the time of the invention would be make multiple, smaller integrated circuits, as taught by Hatada et al.

Regarding claims 6 and 8, Blocker and Hatada et al. together teach the method of claim 5. Blocker further teaches that the second through hole has a straight internal wall and the first size of the first through hole is greater than the second size of the second through hole (see Fig. 3).

Claims 5, 7, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. (U.S. 6,365,513) in view of Hatada et al. (U.S. 4,494,688).

Regarding claim 5, Furukawa et al. teaches a method to manufacture a semiconductor device, comprising preparing a semiconductor wafer including a chip forming section having an electrode (**203** in Fig. 2(a)); forming a first through hole in the electrode (**203a** in Fig. 2(a)); forming a second through hole penetrating the semiconductor wafer and coaxial to the first through hole, the second through hole communicating with the first through hole (hole through wafer **207** in Fig. 2(c) extends

through entire wafer in Fig. 2(e)); and forming a conduction layer (**208** in Fig. 2(e)) that extends via the first and second through holes from a first surface of the semiconductor chip forming section on which the electrode is formed to a second surface opposite the first surface, the conduction layer being electrically connected to the electrode (see Fig. 2(e)).

Furukawa et al. does not teach preparing a semiconductor wafer including a plurality of semiconductor chip forming sections each having an electrode.

Hatada et al. teaches that it is known to prepare a semiconductor wafer including a plurality of semiconductor chip forming sections each having an electrode in the pursuit of miniaturization of integrated circuits (column 1, lines 12-18).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to manufacture a semiconductor device according to the method taught by Furukawa et al. and further fabricate a plurality of such devices, each on its own semiconductor ship forming section with an electrode, as taught by Hatada et al. is common in the semiconductor device processing arts. The motivation for doing so at the time of the invention would be make multiple, smaller integrated circuits, as taught by Hatada et al.

Regarding claim 7, Furukawa et al. and Hatada et al. together teach the method of claim 5. Furukawa et al. further teaches that the first size of the first through hole is the same as the second size of the second through hole (Figs. 2(c) – 2(f)).

Regarding claim 13, Furukawa et al. and Hatada et al. together teach the method of claim 5. Furukawa et al. further teaches that the conduction layer is formed by the plating method (column 8, lines 6-9).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blocker (U.S. 3,969,745) in view of Hatada et al. (U.S. 4,494,688) as applied to claim 5 above, and further in view of Tseng (U.S. 5,843,821).

Blocker and Hatada et al. together teach the method of claim 5, but are silent regarding the method of forming the through hole in the electrode.

Tseng teaches a method of forming a semiconductor device including dry etching a hole in a conductive electrode (column 6, lines 11-21; Fig. 3).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to manufacture a semiconductor device using the method taught by Blocker and Hatada et al. together and according to claim 5, and further, since Tseng teaches that dry etching electrodes yields isotropic etching with straight sidewalls (column 6, line 12; Fig. 3), use this method to etch through the electrode, since the combination of Blocker and Hatada et al. already teaches forming a hole entirely through the electrode.

***Response to Arguments***

Applicant's arguments with respect to claims 5-8, 12, and 13 have been considered but are moot in view of the new ground(s) of rejection.

***Allowable Subject Matter***

Claims 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art does not teach or suggest, in combination with the other claimed limitations, forming a dielectric film covering an electrode and an interior of a first through hole, and forming a through hole penetrating the dielectric film and exposing the electrode, and through which a conduction layer is electrically connected to the electrode.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
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